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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,466	10/31/2000	Shunpei Yamazaki	0756-2222	8851

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,466	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 62-92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 62-92* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 0200* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/784,290.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim1, 3 and 62 – 92 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 3 and 62 – 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Chen, US 5,704,986; Masumo, US 5,306,651 and Takeuchi, US 5,661,056.

Regarding claims 1 and 65, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film comprising amorphous silicon on an insulating surface with reference to Fig. 2 in column 5, line 45;
- providing said semiconductor film with a metal containing material for promoting crystallization of said semiconductor film in between column 4, line 65 and column 5, line1;
- crystallizing said semiconductor film by heating in column 5, line 2;
- irradiating the crystallized semiconductor film with laser light in column 5, line 3.
- forming a semiconductor island having a tapered shape by patterning the semiconductor film having the tapered shape with an angle in the range of 20° to 50° between the side and the underlying surface as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island with reference to Fig. 2C in column 6, lines 20 – 22;

- forming a gate electrode 509 over the semiconductor island with the gate insulating film in between the island and the gate with reference to Fig. 5D in column 7, line 57;
- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;

Suzawa fails to teach: 1) removing the metal from the crystallized semiconductor film by gettering after the irradiation of the laser light, and 2) forming a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide.

Regarding element 1, Chen teaches gettering of metal ions from the semiconductor materials for fabricating transistor devices (see the abstract) for the benefit of saving the device from the degradation effects of impregnated metal ions in column 1, lines 35 – 52.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a gettering treatment after the irradiation of the laser light for the benefit of saving the device from the degradation effects of impregnated metal ions as taught by Chen in column 1, lines 35 – 52.

Regarding element 2, Masumo teaches that during the formation of TFT, a single or a multilayer of silicon oxide and silicon oxide nitride can be made in column 4, lines 1 – 5.

Takeuchi teaches the advantages of multi-layer gate insulating film of oxide and oxide nitride in column 2, lines 21 – 28 since oxide nitride provides good withstand voltage characteristic.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by providing a second gate insulating film of silicon oxide nitride over the first gate insulating film of silicon oxide as taught by Masumo so that the withstand voltage characteristic of the gate is improved as taught by Takeuchi.

Regarding claim 3, Suzawa teaches patterning by an isotropic dry etching method in between column 5, line 61 and column 6, line 13.

Regarding claims 62 and 66, Suzawa teaches that the metal is Ni, Pd, Co, Fe and Pt in column 4, line 67.

Regarding claims 63 and 67, Suzawa fails to teach that gettering is performed by heating the crystallized film in a halogen containing atmosphere.

Chen teaches gettering of metal ions from the semiconductor materials for fabricating transistor devices can be performed in a halogen containing atmosphere (see the abstract) for the benefit of saving the device from the degradation effects of impregnated metal ions in column 1, lines 35 – 52.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device by performing gettering operation by heating the crystallized film in a halogen containing atmosphere for the benefit of saving the device from the degradation effects of impregnated metal ions as taught by Chen in column 1, lines 35 – 52.

Regarding claims 64 and 68, Suzawa fails to teach the surface of the crystallized semiconductor film is oxidized when the gettering is performed.

Chen teaches oxidizing the surface of semiconductor film when gettering is performed (see the abstract) for the benefit of saving the device from the degradation effects of impregnated metal ions in column 1, lines 35 – 52.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's device and perform the oxidation when gettering is performed for the benefit of saving the device from the degradation effects of impregnated metal ions as taught by Chen in column 1, lines 35 – 52.

6. Claims 69 – 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Liu, US 5,147,826 and Chen, US 5,704,986.

Regarding claims 69 and 73, Suzawa teaches a method of making a thin film transistor semiconductor device comprising the steps of:

- forming a semiconductor film comprising amorphous silicon on an insulating surface with reference to Fig. 2 in column 5, line 45;
- providing said semiconductor film with a metal containing material for promoting crystallization of said semiconductor film in between column 4, line 65 and column 5, line1;
- crystallizing said semiconductor film by heating in column 5, line 2;
- irradiating the crystallized semiconductor film with laser light in column 5, line 3.
- patterning the semiconductor film to form a semiconductor island as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island with reference to Fig. 2C in column 6, lines 20 – 22;

- forming a gate electrode 509 over gate insulating film with reference to Fig. 5D in column 7, line 57;
- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;

Suzawa fails to teach: 1) providing a selected portion of the semiconductor film with a metal containing material for promoting crystallization of said semiconductor film; 2) crystallizing said semiconductor film by heating wherein crystallization proceeds from said selected portion in a lateral direction parallel to said insulating surface; and 3) removing the metal from the crystallized semiconductor film by gettering after the irradiation of the laser light.

Regarding elements 1 and 2, Liu teaches providing a selected portion of the semiconductor film with a discontinuous ultra thin film of metal containing materials by providing a relatively low density of nuclei in a uniform background for promoting crystallization of the semiconductor film for the benefit of large grain growth in column 3, lines 57 – 67 and heating the film to crystallize in column 4, lines 35 – 47 on an insulating surface (see Example 1 in column 5) in which the crystallization proceeded inherently from the selected portion in a lateral direction parallel to the insulating surface of the glass to crystallize the whole film.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method by providing a selected portion of the semiconductor film with a metal containing material for promoting crystallization of the semiconductor film and crystallizing said semiconductor film by heating wherein

crystallization proceeds from the selected portion in a lateral direction parallel to the insulating surface for the benefit of large grain growth as taught by Liu in column 3, lines 57 – 67.

Regarding element 3, this limitation has been described earlier in rejecting claims 1 and 65 with reference to Chen.

Regarding claims 70 – 72 and 74 – 76, the limitations of these claims have been described earlier in rejecting claims 62 – 64.

7. Claims 77 – 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Liu, US 5,147,826; Serikawa, US 5,132,754 and Chen, US 5,704,986.

Regarding claims 77 and 81, Suzawa teaches a method of making a semiconductor device comprising the steps of:

- forming a semiconductor film comprising amorphous silicon on an insulating surface with reference to Fig. 2 in column 5, line 45;
- providing said semiconductor film with a metal containing material for promoting crystallization of said semiconductor film in between column 4, line 65 and column 5, line1;
- crystallizing said semiconductor film by heating in column 5, line 2;
- patterning the semiconductor film to form a semiconductor island as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island with reference to Fig. 2C in column 6, lines 20 – 22;

- forming a gate electrode 509 over gate insulating film with reference to Fig. 5D in column 7, line 57;
- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;

Suzawa also teaches laser irradiation of the crystallized semiconductor after the heat annealing. However, Suzawa fails to teach: 1) providing a selected portion of the semiconductor film with a metal containing material for promoting crystallization of said semiconductor film; 2) crystallizing said semiconductor film by heating wherein crystallization proceeds from said selected portion in a lateral direction parallel to said insulating surface; 3) irradiating the crystallized semiconductor film with ultraviolet rays or infrared rays and 4) removing the metal from the crystallized semiconductor film by gettering after the irradiation of the laser light.

Regarding elements 1 and 2, Liu teaches providing a selected portion of the semiconductor film with a discontinuous ultra thin film of metal containing materials by providing a relatively low density of nuclei in a uniform background for promoting crystallization of the semiconductor film for the benefit of large grain growth in column 3, lines 57 – 67 and heating the film to crystallize in column 4, lines 35 – 47 on an insulating surface (see Example 1 in column 5) in which the crystallization proceeded inherently from the selected portion in a lateral direction parallel to the insulating surface of the glass to crystallize the whole film.

Regarding element 3, Serikawa teaches that crystallization of amorphous silicon can be effected also by infrared irradiation instead of the laser irradiation and is therefore functionally equivalent in column 10, lines 30 – 45.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method by replacing the laser irradiation by infrared irradiation as functionally equivalent method taught by Serikawa in column 10, lines 30 – 45.

Regarding element 4, this limitation has been described earlier in rejecting claims 1 and 65 with reference to Chen.

Regarding claims 78 – 80 and 82 - 84, Suzawa in view of Liu and Chen teaches most of the limitations of these claims as have been described in rejecting claims 70 – 72 and 74 – 76.

8. Claims 85 – 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa, US 5,728,259 in view of Serikawa, US 5,132,754 and Chen, US 5,704,986.

Regarding claims 85 and 89, Suzawa teaches a method of making a semiconductor device comprising the steps of:

- forming a semiconductor film comprising amorphous silicon on an insulating surface with reference to Fig. 2 in column 5, line 45;
- providing said semiconductor film with a metal containing material for promoting crystallization of said semiconductor film in between column 4, line 65 and column 5, line1;
- crystallizing said semiconductor film by heating in column 5, line 2;

- patterning the semiconductor film to form a semiconductor island as shown in Fig. 2A in column 6, lines 6 – 9;
- forming a gate insulating film of silicon oxide film on the surface of the semiconductor island with reference to Fig. 2C in column 6, lines 20 – 22;
- forming a gate electrode 509 over gate insulating film with reference to Fig. 5D in column 7, line 57;
- forming source and drain region in the semiconductor island with reference to Fig. 5E in column 8, lines 5 – 10;

Suzawa also teaches laser irradiation of the crystallized semiconductor after the heat annealing. However, Suzawa fails to teach: 1) irradiating the crystallized semiconductor film with ultraviolet rays or infrared rays and 2) removing the metal from the crystallized semiconductor film by gettering after the irradiation of the laser light.

Regarding element 1, Serikawa teaches that crystallization of amorphous silicon can be effected also by infrared irradiation instead of the laser irradiation and is therefore functionally equivalent in column 10, lines 30 – 45.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Suzawa's method by replacing the laser irradiation by infrared irradiation as functionally equivalent method taught by Serikawa in column 10, lines 30 – 45.

Regarding element 2, this limitation has been described earlier in rejecting claims 1 and 65 with reference to Chen.

Regarding claims 86 – 88 and 90 – 92, all limitations have been already discussed earlier in rejecting claims 62 – 64 and 66 – 67 with reference to Suzawa in view of Chen.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571 272 1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
September 20, 2004

Patent Examiner